

Development of Dielectric Resonator Oscillator for Spacecraft Transponding Modem¹

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Abstract — A new Spacecraft Transponding Modem (STM) is being developed by the Jet Propulsion Laboratory for National Aeronautics and Space Administration (NASA) for deep space communication applications. The STM receives an X-band (7.17 GHz) uplink signal and generates an X-band (8.4 GHz) and a Ka-band (32.0 GHz) coherent or noncoherent downlink signals. The STM architecture incorporates three miniature dielectric-resonator-oscillators (DRO). These DROs are used in receiver and exciter frequency synthesis phase-locked loops (PLL) in the STM.

The DROs are designed with custom developed monolithic microwave integrated circuit (MMIC) negative resistance oscillator chips. DROs are laid out on alumina substrates in RF cavity fixtures of 18mm × 18mm × 8mm.

The receiver and the exciter DRO designs meet the following requirements: frequency stability of ± 2 ppm/°C, the free running single-sideband phase noise of - 50 dBc at 1-kHz offset frequency, tuning linearity of $\pm 10\%$ over the ± 1.75 -MHz locking range, and output power of + 10 dBm ± 1 dB over a design temperature range of - 55°C to + 85°C.

The phase-locked loop DRO frequency synthesizers are designed using sampling downconverter and phase detec-

tor MMIC chips. These PLL frequency synthesizers meet the following requirements: pull-in range of ± 1.75 MHz, loop noise bandwidth of 100 kHz, and a single-sideband phase noise of -144 dBc at 1-kHz offset frequency.

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1. INTRODUCTION

This article summarizes the performance results of three DROs developed for deep space Spacecraft Transponding Modem (STM) application [1]. The DROs are used in the

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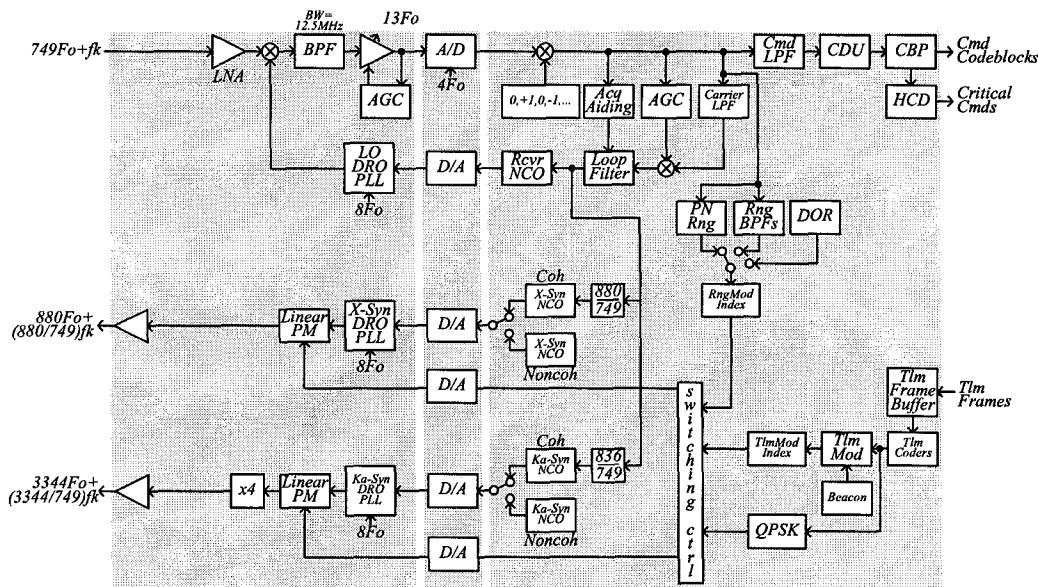


Figure 1. STM Functional Block Diagram

receiver LO DRO-PLL, X-synthesizer DRO-PLL, and Ka-synthesizer DRO-PLL as shown in Figure 1 [1, 2, 3].

Summary of Spacecraft Transponding Modem

The Spacecraft Transponding Modem (STM) implements the standard transponder functions and some of the command and telemetry channel service functions that have previously resided in spacecraft Command and Data Subsystem (CDS). The STM uses custom ASICs, MMICs, and MCM packaging to reduce the active device parts count to 70, mass to 1.5 kg, and volume to 524 cm³.

The STM tracks an X-band uplink signal and provides both X-band and Ka-band downlink signals, either coherent or non-coherent with the uplink signal.

The command detector is integrated into the STM that decodes the uplink commands. The maximum uplink command data rate is 2000 bits per second (bps). The STM implements also a codeblock processor and a hardware command decoder.

Downlink telemetry is received from the spacecraft CDS as telemetry frames. The STM provides the following downlink telemetry coding options: 1) Reed-Solomon coding with interleave depths one and five, 2) the standard convolutional coding with rates (7-1/2) and (15-1/6) used in the Deep Space Network (DSN), and 3) Turbo coding with rates 1/3 and 1/6. The downlink symbol rates can be linearly ramped to match the G/T curve of the receiving

station, providing up to a 1.9 dB increase in data return. Data rates range from 5 bps to 24 Mbps, with three modulation modes provided: 1) modulated subcarrier, 2) bi-phase-L modulated direct on carrier, and 3) Offset-QPSK. Also, the capability to generate one of four non-harmonically related telemetry beacon tones is provided.

Three ranging modes are provided: 1) standard turn around ranging, 2) regenerative pseudo-noise (PN) ranging, and 3) differential one-way ranging (DOR) tone. The regenerative PN-ranging provides the capability of increasing the ground received ranging SNR by up to 30 dB.

Two different avionics interfaces to the CDS data-bus are provided: 1) MIL STD 1553B bus and 2) industry standard PCI interface. Digital interfaces provide the capability to switch between high gain and low gain antennas and to point Ka-band antennas in future missions.

DRO Design Specifications

The design specifications for the DRO and phase lock loop are given in Table 1. The DRO must be capable of generating receiver and exciter local oscillator frequencies of 7 GHz, 8 GHz, and 8.4 GHz. In addition, the DRO must be compact and consume low dc power. The design is to provide +10 dBm buffered output and good phase noise stability. The tolerance on the tuning linearity is ± 7 %. The design approach utilizes custom designed GaAs microwave monolithic integrated circuit (MMIC) negative resistance oscillator in a compact package.

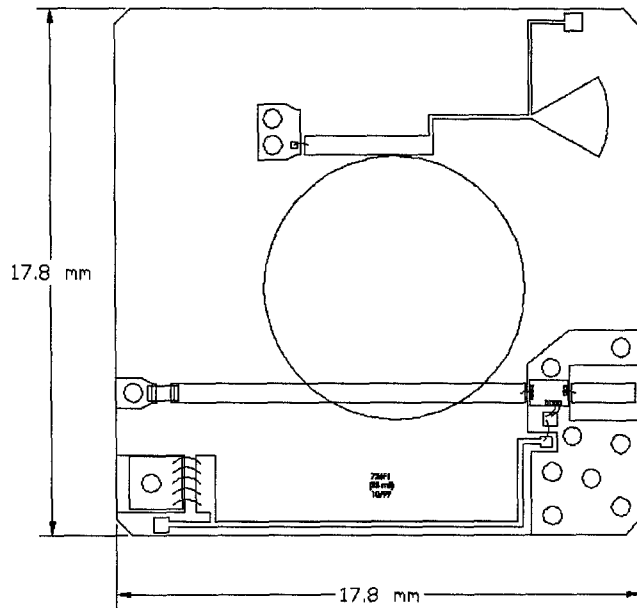


Figure 2. X-Band DRO Layout

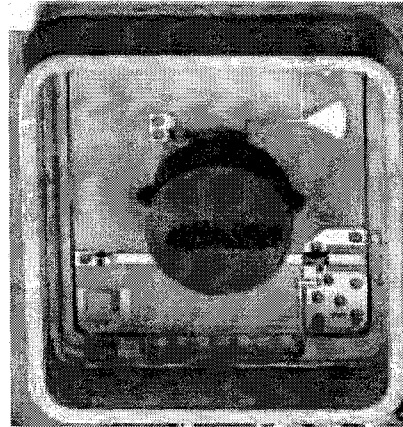


Figure 3. X-Band DRO Picture

Table 1. DRO Design Specifications

Parameter	Value
Chip Size	0.75mm × 1.2mm × 0.1mm
RF Frequency Range	7 GHz - 8.5 GHz
DRO Measured at Frequencies	7 GHz, 8 GHz, and 8.4 GHz
Output Power Level	10.7 dBm ± 0.9 dB
Varactor Tuning Range	± 2 MHz
Tuning Linearity	± 7 %
Free Running SSB Phase Noise Density	- 60 dBc/Hz at 1-kHz offset from carrier
Frequency Stability vs. Temperature	± 2 ppm/°C (max)
Harmonics	- 35 dBc
Spurious	- 80 dBc
DC Current at + 5V DC	30 mA

The organization of the article is as follows. The description of the hybrid DRO configuration is presented in Section 2. The test data, phase-locked loop, and conclusions are presented in Section 3, 4, and 5, respectively.

2. DESCRIPTION OF THE DIELECTRIC RESONATOR OSCILLATOR

The layout of the hybrid X-band receiver DRO [4] is shown in Figure 2. The DRO photograph is shown in Figure 3. It is implemented on a 20-mil thick alumina substrate and dropped into the STM downconverter and synthesizer modules. It consists of a negative resistance

voltage controlled oscillator (VCO) MMIC and two GaAs varactors. The DRO layout size is 17.8 mm × 17.8 mm.

Negative Resistance VCO-MMIC

The negative resistance VCO-MMIC was developed by Hittite Microwave Co., under contract with the NASA Small Business Innovation Research (SBIR) program. The VCO MMIC chip incorporates a negative resistance oscillator along with a buffer amplifier. The MESFET used in this application is a standard 0.5-micron depletion mode MESFET from Triquint (HA2) analog MMIC process. This VCO has been simulated using CAD tools to have large negative resistance over the frequency range of 7 GHz to 8.5 GHz. Two design and fabrication iterations were used to optimize the performance of the VCO chips.

The negative resistance VCO chips, which generate three different DRO frequencies of 7 GHz, 8 GHz, and 8.4 GHz in the STM receiver and exciter, performed well and met all of the specified design goals.

3. MEASURED RESULTS

The measured phase shift versus temperature for the downconverter DRO is shown in Figure 4. The tuning voltage is varied from - 6 V to 0 V for six temperatures from - 45°C to + 75°C.

EM TEST 736FoDRO #1(PUCK 0ppm) vs Temperature

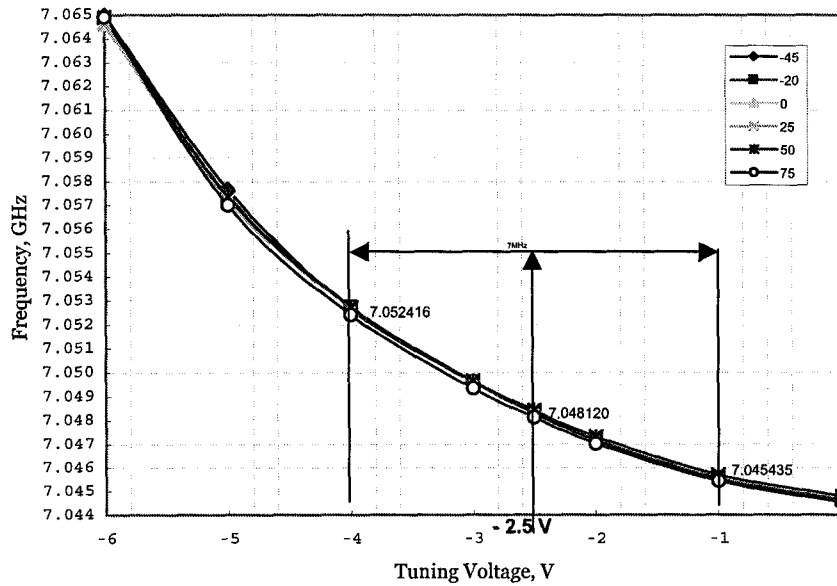


Figure 4. Receiver LO DRO Phase Shift Characteristics with Temperature

The DRO circuit is adjusted by moving the DRO puck to different locations and tuning the RF cavity with a tuning screw that is mounted on the lid to obtain an output frequency of 7048.37 MHz at a dc bias voltage of -2.5 V. The output frequency range is about 7 MHz for a tuning voltage range from -4 V to -1 V.

The DRO output frequency sensitivity is about 2.28 MHz/V at room temperature and varies from 2.25 MHz/V to 2.45 MHz/V for a temperature range of -45°C to $+75^{\circ}\text{C}$.

The DRO output frequency varies from 7048.37 - 0.5 MHz to 7048.37 + 0.25 MHz for a temperature range of -45°C to $+75^{\circ}\text{C}$.

The DRO designs and implementations for the X-band and Ka-band synthesizers are similar to the receiver LO DRO. Their performances are similar also.

4. DRO PHASE-LOCKED LOOP

These DRO drop-in circuits are used in the receiver LO DRO-PLL, X-synthesizer DRO-PLL, and Ka-synthesizer DRO-PLL. The receiver LO DRO-PLL block diagram is shown in Figure 5.

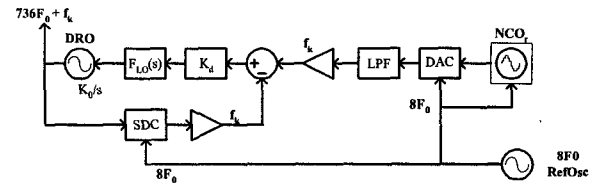


Figure 5. Receiver LO DRO-PLL Block Diagram

The DRO is locked to sum of the NCO output frequency ($f_k = 8.5$ MHz) and the 92nd harmonic of the 8Fo-reference oscillator ($8F_o = 76.5$ MHz). The harmonics of the reference oscillator are generated by a sampling down-converter (SDC) chip.

The phase-noise densities of the reference oscillator and the LO-DRO are shown in Figure 6. For offset-frequencies less than 100 kHz, the phase noise of the DRO is higher than the phase noise of the reference oscillator at $736F_o$. When the DRO is phase-locked to the reference oscillator, the output phase noise improves to that of the reference oscillator within the loop bandwidth as shown in Figure 7. Figure 7 includes the output phase noise for different loop bandwidths. For the receiver LO DRO PLL, the loop bandwidth is chosen to be 100 kHz.

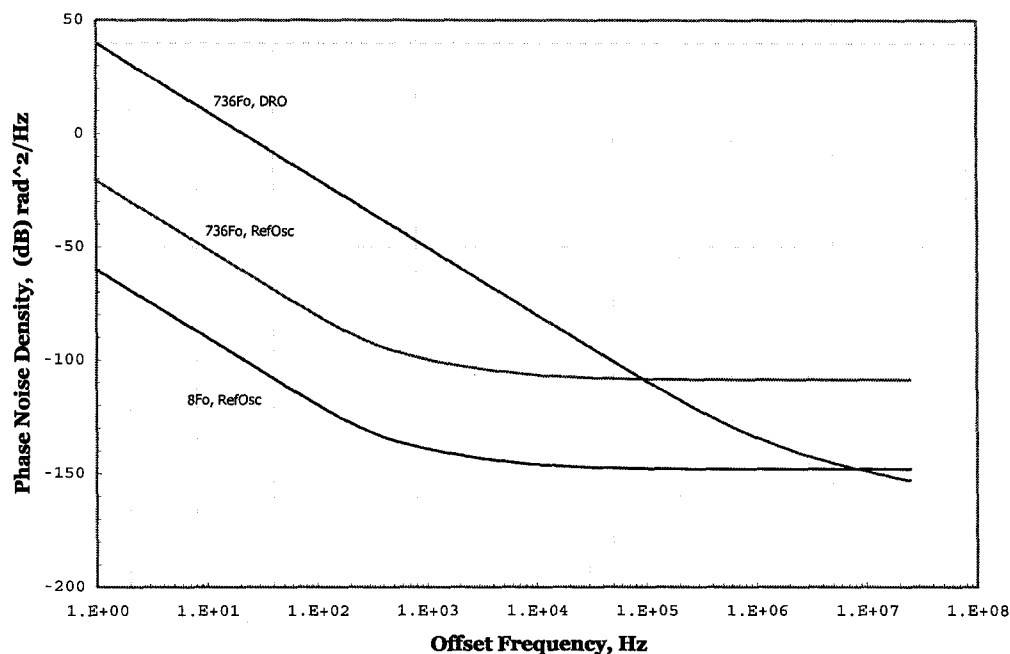


Figure 6. Receiver LO DRO and Reference Oscillator Phase Noise Densities

5. CONCLUSIONS

The DRO design presented is used to generate frequencies from 7 GHz to 8.5 GHz in the STM application. The DRO design used custom GaAs MMIC negative resistance oscillator chips in a very compact package. The DRO output frequency variations due to temperature were compensated using DRO pucks that had opposing temperature coefficients. Thus, the DRO output frequency variations were limited to ± 1 MHz over temperature from -45°C to $+75^{\circ}\text{C}$.

The temperature stability of the DROs simplified the phase-locked loop design for the receiver LO and exciter frequency generation.

6. ACKNOWLEDGEMENT

This DRO design and development for the STM was carried out by the Jet Propulsion Laboratory, California Institute of Technology, under contract with the NASA. The MMIC VCO oscillator research was performed by Hittite Microwave Co., under contract with the NASA Small Business Innovation Research program and under the direction of NASA SBIR center Jet Propulsion Laboratory, California Institute of Technology. The authors

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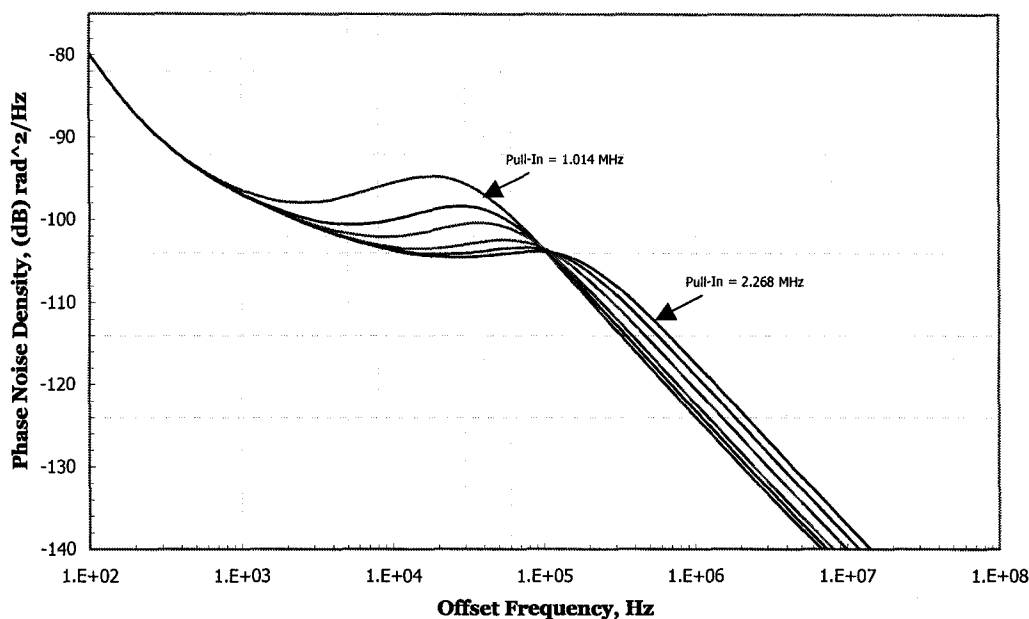
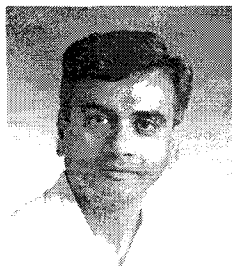


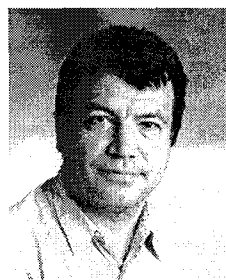
Figure 7. Receiver LO DRO Output Phase Noise Densities for Different Loop Bandwidths



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